

## **SYSTEMS AND METHODS FOR ACTIVELY-PEAKED CURRENT-MODE LOGIC**

### Abstract of the Disclosure

A method and apparatus for creating high speed logic circuits in a CMOS environment using current steering logic cells with actively-peaked NMOS or PMOS loads and the biasing of these logic cells is disclosed. The logic cells can include, for example, buffers, AND gates, OR gates, flip-flops, and latches. The current steering cells with actively-peaked loads can provide benefits such as reduced power consumption, smaller area, and higher speed performance over conventional devices. This performance boost is preferably achieved using NMOS followers with resistively degenerated gates to create frequency peaked transfer function of current-mode logic cells. These logic cells with actively-peaked loads can advantageously be used in circuits in which relatively good power area and performance are desired for state machine logic, parallel to serial conversions, serial to parallel conversions, and the like.

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